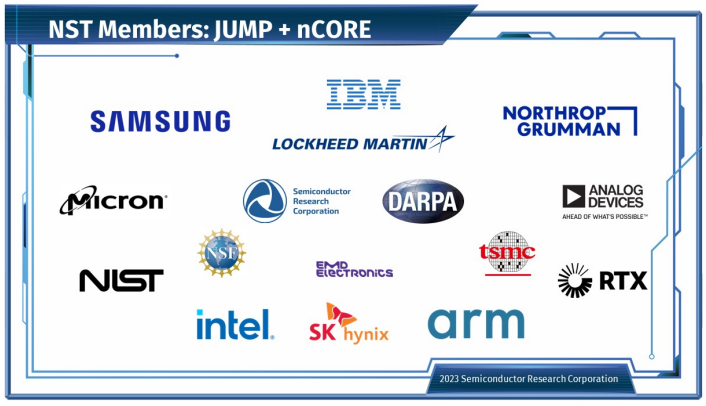
NST PROGRAM RETROSPECTIVE: HIGHLIGHTS AND ACHIEVEMENTS

Semiconductor Research Corporation

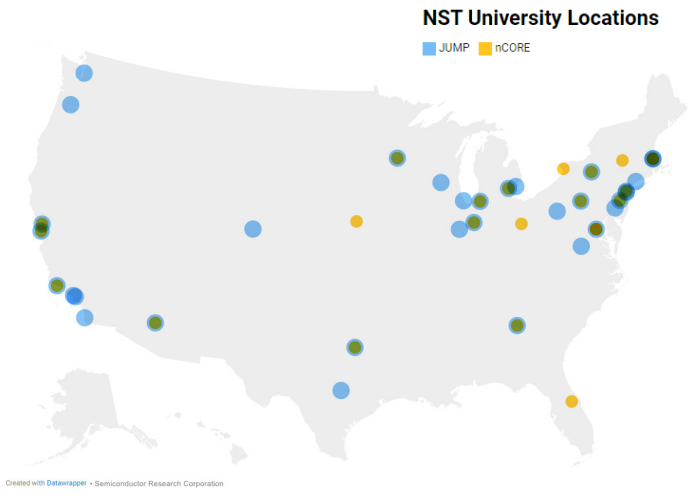
From 2018-2023, Semiconductor Research Corporation initiated and led a public-private partnership called the New Science Team (NST) with a combined investment of over 300 million dollars. Dedicated to a smart, autonomous, safe, connected, efficient, and affordable future, the New Science Team germinated two complementary research programs:

- **Joint University Microelectronics Program (JUMP)** – co-sponsored by commercial and defense industry + DARPA
- **nanoelectronics Computing Research (nCORE)** – co-sponsored by commercial and defense industry + NIST / NSF



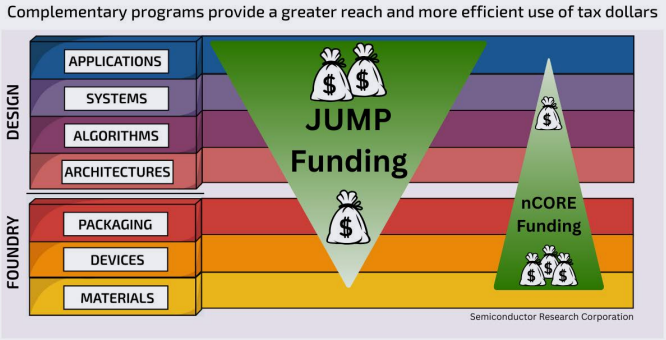
Key Characteristics of NST (JUMP + nCORE)	
Research Management	University-directed
Research	Center and Task based
Time frame	5 Year plan with mid-program adjustments
University Makeup	U.S. Universities
Membership Makeup	International Membership

These two programs funded focused, long-term research at U.S. universities aimed at investing in materials, hardware, design, and novel architectures to move beyond the traditional 2D-scaling paradigm known as "Moore's Law." By leveraging SRC's consortial model, government agencies, industry sponsors, and university researchers pursued the high-risk, high-payoff research needed to address existing and emerging challenges in microelectronic technologies. Solutions were pursued throughout the microelectronics design hierarchy stack, from materials to end applications, and across technology implementation in RF/Analog, Extended CMOS, and Beyond CMOS.



JUMP and nCORE featured some differences that made them perfect partners. JUMP and nCORE allocated funds differently for the various components of the design hierarchy stack. The JUMP program tended to fund "systems research" higher in the stack while the nCORE program tended to fund "device research" as a foundational element for future systems. JUMP was co-funded by DARPA while nCORE was co-funded by NIST and the National Science Foundation. Each program was a collaborative network of focus centers based in over 25 states at 35 and 30 U.S. universities respectively. NST educated at least 1846 students over its years of operation. As of October 2023, NST has concluded operations.

Complementary programs provide a greater reach and more efficient use of tax dollars



The significant achievements resulting from the NST program underscore its remarkable impact.

Program Impact, Since Inception	JUMP	nCORE
Approximate Annual impact ($)	$48 M/yr.	$13 M/yr.
U.S. Universities Represented	35	30
Research Tasks	259	85
Students	1,593	253
Faculty Researchers	168	89
Industrial and Government Liaisons	542	218
Publications	6,224	1,376
Patent Applications to USPTO to date	122	50
Patents Issued by USPTO	22	12

The grand challenges that drove JUMP's mission supported long-term research focused on high performance, energy efficient microelectronics for end-to-end sensing and actuation, signal and information processing, communication, computing, and storage solutions to produce cost-effective, secure, and paradigm-shifting business opportunities. **The research was divided into six topical Centers of Excellence.**

- **ADA Center**
  focused on reigniting system design innovation for advanced architecture and algorithms
- **ASCENT Center**
  focused on foundational materials, devices, and packaging technologies to support heterogeneous integration for the next era of "functional hyper-scaling"
- **CBRIC Center**
  delivered key advances in cognitive computing beyond CPUs, GPUs, and simple Neural Networks (NNs) to enable a new generation of autonomous intelligent systems
- **COMSENTER Center**
  developed technologies for cellular infrastructure using hubs with massive spatial multiplexing and D-band frequencies
- **CONIX Center**
  provided a new middle tier of distributed computing by tightly coupling the cloud and the edge by pushing out autonomy and intelligence into the network using XR as the application driver
- **CRISP Center**
  significantly lowered the programming barrier of effort to achieve highly portable, close-to-the-metal, and understandable performance across a wide range of heterogeneous, intelligent memory architectures, using genomics and personalized medicine as the primary drivers

Conversely, the nCORE program explored fundamental materials, devices, and interconnect solutions to enable future computing and storage paradigms beyond conventional CMOS, beyond von Neumann architecture, and beyond classical information processing/storage. The NEW LIMITS Center had a vertically integrated mission to develop synthesis, integration, and evaluation schemes for new materials for logic, memory, and interconnect applications. The mission of the SMART Center was to accelerate the development of beyond-CMOS building blocks with advanced spintronic materials and devices capable of exponential scaling. Lastly, the IMPACT Center focused on computational modeling with synergistic experimentation to support novel interconnect materials implementable in the medium term to the far future.

The SRC research model, which emphasizes cooperative collaboration, is remarkable. The NST program produced >10,000 documented interactions between industry and academia that resulted in >200 instances of meaningful technology transfer. Here are some standout examples:

"CHIPKIT," an agile and reusable open-source framework that provides basic IO, an on-chip programmable host, off-chip hosting, memory, and peripherals and is accelerating test chip development and validation.

"NeuroSim," an integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures. It is a circuit-level model for benchmarking neuro-inspired architectures based on CMOS and emerging memories.

A 140 GHz massive MIMO hub, picocell, and handset array that validates the principle of demonstrator platforms and is establishing itself as a leading testbed for 6G system research in communications and sensing.

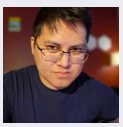
"ARENA," an Augmented Reality Edge Networking Architecture that is quickly becoming a platform for real-time XR interaction between multiple users and the physical world.

Thought leadership that has resulted in SRC's 2030 Decadal Plan for Semiconductors. The five seismic shifts outlined in the Decadal Plan give researchers a clear plan on the important problems to solve today.

Lived research experience that has informed SRC's recently published Microelectronics and Advanced Packaging Technologies Roadmap, which aims to develop the packaging ecosystem to support new chip, chiplet and SiP technologies while enabling the workforce development of the next generation of semiconductor workers.

The World's 1st Embedded Die with D-Band Integrated Antenna in a Glass Interposer was developed by Madhavan Swaminathan's group in JUMP's ComSenTer and ASCENT centers. This research graduated to the next level through its inclusion in Qorvo's RF Packaging program, SHIP (State-of-the-Art Heterogeneous Integrated Packaging).

Beyond the research results, NST had a significant impact on workforce development. NST educated at least 1846 students over its years of operation. Here are some stellar NST students.



Onri Jay Benally, pursuing PHD in Electrical Engineering (2027) at University of Minnesota; Participated in nCORE SMART Center.

Dr. Aristide Gumyusenge, PHD in Chemistry (2019) from Purdue University; Currently Assistant Professor at MIT; participated in nCORE IMPACT Center.

Dr. Mohsen Imani, PHD in Computer Science and Engineering (2020) from UC San Diego; currently Assistant Professor at UC Irvine; participated in JUMP CRISP Center.

Dr. Isha Datye, PHD in Electrical Engineering (2020) from Stanford University; Currently Principal Engineer at TSMC; participated in JUMP ASCENT Center.

Dr. Joonseop Sim, PHD in Electrical Engineering (2020) from UC San Diego; Currently Principal Engineer at SK hynix; participated in JUMP CRISP Center.